REMARKS

Claims 1-15 were presented for examination. Claims 1 and 7 were rejected, and claims 2-6 and 8-15 were objected to but deemed allowable.

The applicants have canceled claims 1 and 7 and have amended claims 2-6 and 8-15 as suggested, and, therefore the applicants respectfully request consideration in light of the above amendments and the following comments.

35 U.S.C. 102 Rejection of Claims 1 and 7

Claims 1 and 7 were rejected under 35 U.S.C. 102(e) as being anticipated by T. Sowlati, U.S. Patent 6,515,547 (hereinafter "Sowlati"). Claims 1 and 7 have been canceled. The limitations of claim 1 have been incorporated into newly independent claims 2 and 3, and the limitations of claim 7 have been incorporated into newly independent claims 8 and 9. The applicants respectfully submit that the pending claims, as amended, overcome the rejection.

Claim 2, as amended, recites:

> 2. An apparatus comprising:
>
> a first transistor having a gate terminal, a drain terminal, and a source terminal;
>
> a first resistor having a first terminal and second terminal, wherein said first terminal of said first resistor is electrically connected to said gate terminal of said first transistor;
>
> a second transistor having a gate terminal, a drain terminal, and a source terminal, wherein said drain terminal of said second transistor is electrically connected to said source terminal of said first transistor; and
>
> a second resistor having a first and a second terminal, wherein said first terminal of said second resistor is electrically connected to said gate terminal of said second transistor, and wherein said second terminal of said second resistor is electrically connected to said drain terminal of said first transistor;
>
> *wherein a first voltage connected to said second terminal of said first resistor is greater than a second voltage connected to said drain terminal of said first transistor by at least the gate-to-source threshold voltage of said first transistor.*
>
> (*emphasis supplied*)

Nowhere does Sowlati teach or suggest, alone or in combination with the other references, what claim 2 recites – namely the voltage connected to the second terminal of

the first resistor is greater than the voltage connected to the drain of the first transistor by at least the gate-to-source threshold of the *first* transistor. For this reason, the applicants respectfully submit that claim 2 is allowable.

Claim 3, as amended, recites:

> 3. An apparatus comprising:
>
> a first transistor having a gate terminal, a drain terminal, and a source terminal;
>
> a first resistor having a first terminal and second terminal, wherein said first terminal of said first resistor is electrically connected to said gate terminal of said first transistor;
>
> a second transistor having a gate terminal, a drain terminal, and a source terminal, wherein said drain terminal of said second transistor is electrically connected to said source terminal of said first transistor; and
>
> a second resistor having a first and a second terminal, wherein said first terminal of said second resistor is electrically connected to said gate terminal of said second transistor, and wherein said second terminal of said second resistor is electrically connected to said drain terminal of said first transistor;
>
> *wherein said first transistor further comprises a first substrate terminal and said second transistor further comprises a second substrate terminal wherein said first substrate terminal and said second substrate terminal are electrically connected to each other.*
>
> (*emphasis supplied*)

Nowhere does Sowlati teach or suggest, alone or in combination with the other references, what claim 3 recites – namely the arrangement of the first and second transistors and that the substrate terminals of the first and second transistors are electrically connected to each other. For this reason, the applicants respectfully submit that claim 3 is allowable.

Because claims 4 through 6 depend on claim 3, the applicants respectfully submit that they are also allowable.

Claim 8, as amended, recites:

> 8. An apparatus comprising:
>
> a first transistor having a gate terminal, a drain terminal, and source terminal;
>
> a second transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said first transistor is electrically connected to said drain terminal of said second transistor;

> a first resistor having a first terminal and second terminal, wherein said first terminal of said first resistor is electrically connected to said gate terminal of said first transistor;
>
> a second resistor having a first terminal and second terminal, wherein said first terminal of said second resistor is electrically connected to said drain terminal of said second transistor, and wherein said second terminal of said second resistor is electrically connected to said gate terminal of said second transistor;
>
> *a third transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said third transistor is electrically connected to said source terminal of said second transistor, and wherein said drain terminal of said third transistor is electrically connected to said first terminal of said second resistor;*
>
> *a fourth transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said fourth transistor is electrically connected to said drain terminal of said third transistor, and wherein said drain terminal of said fourth transistor is electrically connected to said drain terminal of said first transistor; and*
>
> a third resistor having a first terminal and second terminal, wherein said first terminal of said third resistor is electrically connected to said gate terminal of said fourth transistor, and wherein said second terminal of said third resistor is electrically connected to said second terminal of said first resistor.
>
> (*emphasis supplied*)

Nowhere does Sowlati teach or suggest, alone or in combination with the other references, what claim 8 recites – namely the inclusion of the third and fourth transistors. For this reason, the applicants respectfully submit that claim 8 is allowable.

Because claims 10 through 15 depend on claim 8, the applicants respectfully submit that they are also allowable.

Claim 9, as amended, recites:

> 9. An apparatus comprising:
>
> a first transistor having a gate terminal, a drain terminal, and source terminal;
>
> a second transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said first transistor is electrically connected to said drain terminal of said second transistor;
>
> a first resistor having a first terminal and second terminal, wherein said first terminal of said first resistor is electrically connected to said gate terminal of said first transistor; and
>
> a second resistor having a first terminal and second terminal, wherein said first terminal of said second resistor is electrically connected to said drain terminal of said second transistor, and wherein said second terminal of said

second resistor is electrically connected to said gate terminal of said second transistor;

wherein a first voltage connected to said second terminal of said first resistor is greater than a second voltage connected to said drain terminal of said first transistor by at least the gate-to-source threshold voltage of said first transistor.

(*emphasis supplied*)

Nowhere does Sowlati teach or suggest, alone or in combination with the other references, what claim 9 recites – namely that the voltage of the second terminal of the first resistor is greater than the voltage of the drain of the first transistor by at least the gate-to-source threshold voltage of the first transistor. For this reason, the applicants respectfully submit that claim 9 is allowable.

The applicants respectfully object to the Office's definition of the term "electronically connected" as used in the Office action.

The Office action contends that the phrase "electrically connected" should be "broadly interpreted to include a connection which allows intervening elements" including a resistor, capacitor, or inductor and, therefore, two nodes connected by a resistor, capacitor, or inductor anticipate a recitation of two nodes connected by a (theoretically) non-resistive and non-reactive lead. The applicant respectfully disagrees.

First, the applicant respectfully submits that the Office's interpretation is in direct conflict with the usage of the term as used by those of ordinary skill in the art at the time that the invention was made.

The applicant submits that "electrically connected", "connected", and "tied" are used in the applicant's specification to describe each connection that is a short between points (*i.e.*, the points are at the same electrical potential for any current). The term, "electrically connected," as used in the specification to describe such interconnection, is consistent with common usage in electrical engineering circuit analysis.

Second, the applicant respectfully submits that the Office's interpretation, if accepted, renders the verbal description of circuit connectivity meaningless.

The Office action asserts that "electrically connected" is broadly interpreted as a connection that allows intervening elements. Such an interpretation, however, renders the verbal description of electrical interconnectivity impossible. If the Office action's interpretation were accepted, every node in a circuit is "electrically connected" to every other node, and a resistive network would be indistinguishable from a single wire.

For example, Figure 1 depicts two circuits that are equivalent if one were to apply the Office's interpretation of the term "electrically connected." In each case, node A would be considered electrically connected to node B. The two circuits are, of course, quite different.

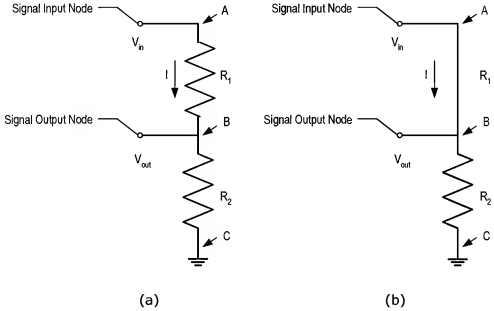

Figure 1: *(a) and (b) depict two circuits that are equivalent if the broad interpretation of the term "electrically connected" is applied.*

The conclusion that (1) "electrically connected" allows for intervening elements, the applicant respectfully submits, is untenable.

Request for Reconsideration Pursuant to 37 C.F.R. 1.111

Having responded to each and every ground for objection and rejection in the Office action mailed May 19, 2006, applicants request reconsideration of the instant application pursuant to 37 CFR 1.111 and request that the Examiner allow all of the pending claims and pass the application to issue.

Should there remain unresolved issues the applicants respectfully request that Examiner telephone the applicants' attorney at 732-578-0103 x11 so that those issues can be resolved as quickly as possible.

Respectfully,
Nasir Abdul Quadir et al.

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